Remarks

Claims 1, 4-12, and 14-18, 20, and 21 remain pending in the application. Claims 1, 8, and 18 are amended by the foregoing amendment, and claims 2, 3, 13, and 19 are Cancelled, rendering the rejection of those claims moot.

Claims 1-5 and 18-20 are rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 6,829,683 (Kuskin). Applicants traverse this rejection as to claims 1, 4, 5, 18, and 20.

Kuskin discloses transferring ownership of data in a distributed shared memory system, but does not disclose or suggest the claimed invention. In Kuskin, a first processor requesting the return of a modified cache line sends a return request to a processor interface, which forwards it to a memory directory associated with a second processor. The memory directory generates an intervention request to the processor interface. An intervention response is generated in response to the intervention request and is sent from the processor interface to the second processor before the return request is processed. The intervention response includes the cache line.

In the present invention, a first processor requests ownership of a cache line from a memory unit. The memory unit determines which of a plurality of other processors has ownership of the requested cache line and sends a recall to that processor. In response to the recall, the second processor sends the requested cache line to the first processor. A response transaction is sent from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor, and a response transaction is sent from the processor with ownership to the memory unit to confirm that the processor with ownership has sent the requested cache line to the first processor. These latter two transactions ensure that the first cache-to-cache transfer is complete before the memory unit can launch another intervention request.

In Kuskin, cache line data is sent from one processor to another. However, Kuskin does not disclose or suggest sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor, and sending a response transaction from the processor with ownership to the memory unit to confirm that the processor with ownership has sent the requested cache line to the first processor. Thus, Kuskin cannot anticipate claims 1 (as amended), 4, 5, 18 (as amended), and 20, and the rejection under 35 U.S.C. § 102(e) should be withdrawn.

Claims 6, 7, 17, and 21 are rejected under 35 U.S.C. § 103(a) over Kuskin in combination with U.S. patent 6,981,106 (Bauman). Applicants traverse this rejection.

As noted above, Kuskin fails to suggest sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor, and sending a response transaction from the processor with ownership to the memory unit to confirm that the processor with ownership has sent the requested cache line to the first processor. Bauman likewise fails to suggest this feature. While Bauman may suggest, *arguendo*, updating a memory tag, the combination of Kuskin and Bauman still fails to suggest sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor, and sending a response transaction from the processor with ownership to the memory unit to confirm that the processor with ownership has sent the requested cache line to the first processor. Since Bauman fails to supply a feature missing from Kuskin, the combination of Kuskin and Bauman cannot suggest the invention and cannot render claims 6, 7, 17, and 21 obvious. This rejection is, therefore, without foundation and should be withdrawn.

Claims 8-16 are rejected under 35 U.S.C. § 103(a) over Kuskin in combination with U.S. patent 6,381,681 (McCracken). As with the combination of Kuskin and Bauman, the combination of Kuskin and McCracken does not yield a method in which a cache line is sent from one processor directly to another in response to a recall request, followed by a response transaction sent from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor, and a response transaction sent from the processor with ownership to the memory unit to confirm that the processor with ownership has sent the requested cache line to the first processor. While McCracken may disclose a shared memory processor system, it lacks any suggestion of sending a cache line directly from one processor to another, followed by a response transaction sent from the first processor to the memory unit and a response transaction sent from the processor with ownership to the memory unit. Consequently, the combination of Kuskin and McCracken cannot render claims 8 (as amended) to 12 and 14-16 obvious, and the rejection of claims 8 (as amended) to 12 and 14-16 should be withdrawn.

CONCLUSION

Based upon the foregoing amendments and remarks, the application is believed to be in condition for allowance. Withdrawal of all rejections and objections, and an early notice of allowance of claims 1-21 is earnestly solicited.

Respectfully submitted,

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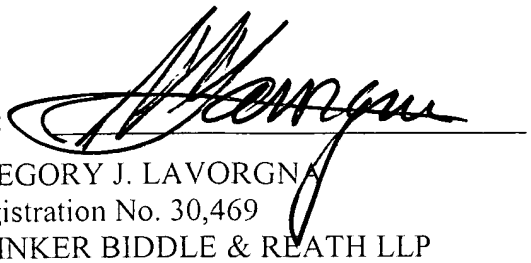
BY: 

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